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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GUILL, RUSSELL L	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/920,382	VENKITAKRISHNAN, PADMANABHA	
	Examiner	Art Unit	
	Russell L. Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/31/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~4/2/02~~ 2 pages
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 23 have been examined. Claims 1 – 23 have been rejected.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claim 2, line 23 recites "delineates power consumption of said is in terms of maximum power". The phrase appears to have extra words. For the purpose of claim interpretation, the phrase is interpreted as "delineates power consumption in terms of maximum power".

4. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claim 12, the claim recites, "inserting said power weight into said instruction stream at a corresponding appropriate place therein". The Examiner does not understand how a power weight is inserted into an instruction stream. For

the purpose of claim evaluation, the phrase is interpreted as "inserting said power weight into the appropriate place in the functional model".

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claim 1 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 10 of U.S. Patent No. 6,513,145. Although the conflicting claims are not identical, they are not patentably distinct from each other because they describe the equivalent function and structure.

6.1. Both the application claim 1 and the patent claim 10 have five steps. Steps 1, 2, 4, and 5 of the application claim 1 are identical to the steps 1, 2, 4, and 5 of the patented claim 10.

6.2. Step 3 of the application claim 1 is "valuating a power weight for each stage of each said function of each said constituent", which is similar to step 3 of the patent claim 10, "adding a power weight for each said stage of each said function".

6.3. The definition of "valuate" is "to place a value on", therefore, "valuating a power weight for each said stage" is equivalent to "adding a power weight for each said stage". Also, the effect of both step 3 of the application and step 3 of the patent is to assign a power weight to all stages of the electronic architecture. Therefore, both step 3 of the application and step 3 of the patent are obviously functionally equivalent.

6.4. Although the conflicting claims are not identical, they are not patentably distinct from each other because they describe the equivalent function and structure.

7. Claim 2 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 11 of U.S. Patent No. 6,513,145. Although the conflicting claims are not identical, they are not

patentably distinct from each other because they describe the equivalent function and structure.

7.1. Application claim 2 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

7.2. Patent claim 11 is a dependent claim of claim 10, and thereby inherits all of the limitations of claim 10.

7.3. Both the application claim 2 and the patent claim 11 have a single step. The only difference is at the end of both claims. The application claim 2 ends with "wherein said benchmark delineates power consumption of said is in terms of maximum power." The patent claim 11 ends with "wherein said power consumption is in terms of maximum power." These phrases are obviously functionally equivalent.

8. Claim 3 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 12 of U.S. Patent No. 6,513,145. Although the conflicting claims are not identical, they are not patentably distinct from each other because they describe the equivalent function and structure.

8.1. Application claim 3 is a dependent claim of claim 2, and thereby inherits all of the rejected limitations of claim 2.

8.2. Patent claim 12 is a dependent claim of claim 11, and thereby inherits all of the limitations of claim 11.

8.3. The words of patent claim 12 are identical to application claim 3. The only differences are in the parent claims, as discussed above. Therefore, the claims are obviously functionally equivalent.

9. Claim 4 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 13 of U.S. Patent No. 6,513,145. Although the conflicting claims are not identical, they are not patentably distinct from each other because they describe the equivalent function and structure.

9.1. Application claim 4 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

9.2. Patent claim 13 is a dependent claim of claim 10, and thereby inherits all of the limitations of claim 10.

9.3. Both the application claim 4 and the patent claim 13 have a single step. The only difference is that the application claim 4 recites "wherein compiling said benchmark program", and the patent claim 13 recites "wherein compiling a benchmark program". These phrases are obviously functionally equivalent.

10. Claim 5 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 14 of U.S. Patent No. 6,513,145. Although the conflicting claims are not identical, they are not patentably distinct from each other because they describe the equivalent function and structure.

10.1. Application claim 5 is a dependent claim of claim 4, and thereby inherits all of the rejected limitations of claim 4.

10.2. Patent claim 14 is a dependent claim of claim 13, and thereby inherits all of the limitations of claim 13.

10.3. The words of patent claim 14 are identical to application claim 5. The only differences are in the parent claims, as discussed above. Therefore, the claims are obviously functionally equivalent.

11. Claim 6 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 15 of U.S. Patent No. 6,513,145. Although the conflicting claims are not identical, they are not patentably distinct from each other because they describe the equivalent function and structure.

11.1. Application claim 6 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

11.2. Patent claim 15 is a dependent claim of claim 10, and thereby inherits all of the limitations of claim 10.

11.3. The steps of both application claim 6 and the patent claim 15 have the identical. The only difference is in the preamble. The application claim 6 preamble recites "wherein said valuating a power weight for each said stage of each said function of each said constituent", and the patent claim 15 preamble recites "wherein said adding a power weight for each said stage of each said function". The effect of both of these phrases is to assign a power weight to all stages. Therefore, these phrases are obviously functionally equivalent.

12. Claim 7 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 16 of U.S. Patent No. 6,513,145. Although the conflicting claims are not identical, they are not patentably distinct from each other because they describe the equivalent function and structure.

12.1. Application claim 7 is a dependent claim of claim 6, and thereby inherits all of the rejected limitations of claim 6.

12.2. Patent claim 16 is a dependent claim of claim 15, and thereby inherits all of the limitations of claim 15.

12.3. The words of patent claim 16 are identical to application claim 7. The only differences are in the parent claims, as discussed above. Therefore, the claims are obviously functionally equivalent.

13. Claim 8 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 17 of U.S. Patent No. 6,513,145. Although the conflicting claims are not identical, they are not patentably distinct from each other because they describe the equivalent function and structure.

13.1. Application claim 8 is a dependent claim of claim 6, and thereby inherits all of the rejected limitations of claim 6.

13.2. Patent claim 17 is a dependent claim of claim 15, and thereby inherits all of the limitations of claim 15.

13.3. The words of patent claim 17 are identical to application claim 8. The only differences are in the parent claims, as discussed above. Therefore, the claims are obviously functionally equivalent

14. Claim 9 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 18 of U.S. Patent No. 6,513,145. Although the conflicting claims are not identical, they are not patentably distinct from each other because they describe the equivalent function and structure.

14.1. Application claim 9 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

14.2. Patent claim 18 is a dependent claim of claim 10, and thereby inherits all of the limitations of claim 10.

14.3. Both the application claim 9 and the patent claim 18 have a single step. The only difference is that the application claim 4 recites, "wherein said running said model in a maximum power consumption mode comprises running a power virus program", and the patent claim 18 recites, "wherein said summarizing said power consumption further comprises running a power virus program". The effect of both of these phrases would result in the same summary of power consumption. Therefore, these phrases are obviously functionally equivalent.

15. Claim 10 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 19 of U.S. Patent No. 6,513,145. Although the conflicting claims are not identical, they are not patentably distinct from each other because they describe the equivalent function and structure.

15.1. Application claim 10 is a dependent claim of claim 1, and thereby inherits all of the rejected limitations of claim 1.

15.2. Patent claim 19 is a dependent claim of claim 10, and thereby inherits all of the limitations of claim 10.

15.3. The words of patent claim 10 are identical to application claim 10. The only differences are in the parent claims, as discussed above. Therefore, the claims are obviously functionally equivalent.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (Chen, Rita Yu; Irwin, Mary Jane; Raminder, S. Bajwa; "An Architectural Level Power Estimator", 1998, ISCA 1998) in view of Fornaciari (Fornaciari, W.; Gubian, P.; Sciuto, D.; Silvano, C.; "System-Level Power Evaluation Metrics", 1997, Proceedings, Second Annual IEEE International Conference on Innovative Systems in Silicon 1997).

17.1. The art of Chen is directed toward architectural level power estimation ***(Title)***.

17.2. The art of Fornaciari is directed to high-level power estimation that operates at the architectural level ***(Abstract)***.

17.3. Chen appears to teach determining a benchmark for power consumption by an architecture and architectural functions ***(section 3.0 Validation, paragraphs 1 – 3, and page 3, figure 3 and table 2)***.

17.4. Chen appears to teach specifying a design analysis to be performed ***(section 3.0 Validation, paragraphs 1 – 3, and page 3, figure 3 and table 2)***.

17.4.1. Regarding ***(section 3.0 Validation, paragraphs 1 – 3, and page 3, figure 3 and table 2)***; it is obvious that a design analysis is specified when each benchmark program is run since each benchmark program tests a different set of architectural features.

17.5. Chen appears to teach summarizing a resulting operation into a summary ***(figure 4 and figure 5)***.

17.5.1. Regarding ***(figure 4 and figure 5)***; the figures are obviously summaries of operations.

17.6. Chen does not specifically teach:

17.6.1. selecting one of the functions

17.6.2. designating one of the stages constituting one of the functions selected

17.6.3. removing a set of instruction set architecture instructions corresponding to one of the stages designated

17.6.4. emulating the constituent subfunction corresponding to one of the stages designated

17.7. Fornaciari appears to teach ***(page 325, section 2. Metric Driven System-Level Partitioning, paragraph 1)***:

17.7.1. selecting one of the functions

17.7.2. designating one of the stages constituting one of the functions selected

17.7.3. removing a set of instruction set architecture instructions corresponding to one of the stages designated

17.7.4. emulating the constituent subfunction corresponding to one of the stages designated

17.8. Regarding ***(page 325, section 2. Metric Driven System-Level Partitioning, paragraph 1) above;*** it is obvious that moving

operations from the hardware (HW) side to the software (SW) side performs the operations listed above.

17.9. Chen and Fornaciari are analogous art because they are both directed to the same problem area of architectural level power estimation.

17.10. The motivation to combine the art of Fornaciari with the art of Chen would have been obvious given the need expressed in Chen for a tool for architectural level power estimation ***(section 1.0 Introduction, first paragraph)***, and the solutions described in Fornaciari.

17.11. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Fornaciari with the art of Chen to produce the invention of claim 11.

18. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (Chen, Rita Yu; Irwin, Mary Jane; Raminder, S. Bajwa; "An Architectural Level Power Estimator", 1998, ISCA 1998) and Fornaciari (Fornaciari, W.; Gubian, P.; Sciuto, D.; Silvano, C.; "System-Level Power Evaluation Metrics", 1997, Proceedings, Second Annual IEEE International Conference on Innovative Systems in Silicon 1997) in view of Landman (Landman, Paul; High-Level Power Estimation", 1996, International Symposium on Low Power Electronics and Design, Proceedings of the 1996 International Symposium on Low Power Electronics and Design).

18.1. Claim 12 is a dependent claim of claim 11, and thereby inherits all of the rejected limitations of claim 11.

18.2. The art of Chen is directed toward architectural level power estimation ***(Title)***.

18.3. The art of Landman is directed to high-level power estimation that operates at the architectural, behavior, instruction, and system levels ***(Abstract)***.

18.4. Chen appears to teach modeling a functional model of an architecture ***(section 2.0 Power Estimation, paragraphs 1 – 3, and page 2, figure 1 Power Estimator Overview, and section 1.0 Introduction, paragraph 4)***.

18.5. Chen appears to teach compiling a benchmark program into a corresponding instruction stream ***(section 2.0 Power Estimation, paragraphs 1 – 3, and page 2, figure 1 Power Estimator Overview, and section 1.0 Introduction, paragraph 4)***.

18.5.1. Regarding ***(section 2.0 Power Estimation, paragraphs 1 – 3, and page 2, figure 1 Power Estimator Overview, and section 1.0 Introduction, paragraph 4)***; it is obvious that the assembler compiles the program into instructions.

18.6. Chen appears to teach running a functional model to determine the power consumption ***(section 2.0 Power Estimation, paragraphs 1 – 3, and page 2, figure 1 Power Estimator Overview, and section 1.0 Introduction, paragraph 4)***.

18.6.1. Regarding ***(section 2.0 Power Estimation, paragraphs 1 – 3, and page 2, figure 1 Power Estimator Overview, and section 1.0 Introduction, paragraph 4)***; it would have been obvious to one of ordinary skill in the art at the time of invention to run the model in maximum power consumption mode.

18.7. Chen appears to teach inserting the power weight into the instruction stream at a corresponding appropriate place therein ***(section 2.0 Power Estimation, all paragraphs, and figure 1)***.

18.7.1. Regarding ***(section 2.0 Power Estimation, all paragraphs, and figure 1);*** it is obvious that power weights are inserted into the appropriate functional unit in figure 1 since energy consumed is associated with each functional unit.

18.8. Chen appears to teach summarizing the power consumption ***(page 2, figure 1 Power Estimator Overview, item Power Consumption Output, and section 1.0 Introduction, paragraph 4)***.

18.9. Chen does not specifically teach valuating a power weight for each stage of each function of each constituent of an electronic architecture.

18.10. Landman appears to teach valuating a power weight for each stage of each function of each constituent of an electronic architecture ***(section 3.1.1 Complexity-based models, especially equation 1)***.

18.11. Chen and Landman are analogous art because they are both directed to the same problem area of architectural level power estimation.

18.12. The motivation to combine the art of Landman with the art of Chen would have been obvious given the need expressed in Chen for a tool for architectural level power estimation ***(section 1.0 Introduction, first paragraph)***, and the solutions described in Landman.

18.13. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Landman with the art of Chen and Fornaciari to produce the invention of claim 12.

19. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (Chen, Rita Yu; Irwin, Mary Jane; Raminder, S. Bajwa; "An Architectural Level Power Estimator", 1998, ISCA 1998) and Fornaciari (Fornaciari, W.; Gubian, P.; Sciuto, D.; Silvano, C.; "System-Level Power Evaluation Metrics", 1997, Proceedings, Second Annual IEEE International

Conference on Innovative Systems in Silicon 1997) and Landman (Landman, Paul; High-Level Power Estimation", 1996, International Symposium on Low Power Electronics and Design, Proceedings of the 1996 International Symposium on Low Power Electronics and Design) in view of Bartleson (Bartleson, Karen "A New Standard for System-Level Design", September 1999).

19.1. Claim 13 is a dependent claim of claim 12, and thereby inherits all of the rejected limitations of claim 12.

19.2. The art of Bartleson is directed to using SystemC for modeling concepts at the system level and behavior level ***(page 2, section "SystemC" Defined)***.

19.3. Bartleson appears to teach modeling a functional model of an architecture by writing a program in SystemC ***(page 2, paragraph 4, and section "SystemC" Defined)***.

19.4. Bartleson and Chen are analogous art because they all have the common problem of modeling concepts at the architectural level.

19.5. The motivation to combine the art of Bartleson with the art of Chen would have been obvious given the target use of SystemC for hardware modeling concepts at the system, behavioral and register transfer level, expressed in Bartleson ***(section "SystemC" Defined)***.

19.6. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Bartleson with the art of Chen and Landman and Fornaciari to produce the invention of claim 13.

20. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (Chen, Rita Yu; Irwin, Mary Jane; Raminder, S. Bajwa; "An Architectural Level Power Estimator", 1998, ISCA 1998) and Fornaciari (Fornaciari, W.; Gubian, P.; Sciuto, D.; Silvano, C.; "System-Level Power Evaluation Metrics", 1997, Proceedings, Second Annual IEEE International Conference on Innovative Systems in Silicon 1997) and Landman (Landman, Paul; High-Level Power Estimation", 1996, International Symposium on Low Power Electronics and Design, Proceedings of the 1996 International Symposium on Low Power Electronics and Design) in view of ComputerDictionary ("Computer Dictionary", 1994, Microsoft Press).

20.1. Claim 14 is a dependent claim of claim 12, and thereby inherits all of the rejected limitations of claim 12.

20.2. The art of ComputerDictionary is directed to common knowledge of the ordinary artisan.

20.3. Chen does not specifically teach compiling a benchmark into a corresponding instruction stream by a compiler.

20.4. ComputerDictionary appears to teach compiling a computer program into a corresponding instruction stream by a compiler ***(page 85 – 86, entry for "compiler")***.

20.5. Therefore, as discussed above, it was common knowledge of the ordinary artisan at the time of invention that a compiler was used to compile a computer program into a corresponding instruction stream.

20.6. Chen and ComputerDictionary are analogous art because they both contain the problem of compiling a computer program into a corresponding instruction stream.

20.7. The motivation to use the art of Chen with the art of ComputerDictionary would have been obvious because a compiler is normally used to convert a computer program into a corresponding instruction stream.

20.8. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of ComputerDictionary with the art of Chen to produce the invention of claim 14.

21. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (Chen, Rita Yu; Irwin, Mary Jane; Raminder, S. Bajwa; "An Architectural Level Power Estimator", 1998, ISCA 1998) and Fornaciari

(Fornaciari, W.; Gubian, P.; Sciuto, D.; Silvano, C.; "System-Level Power Evaluation Metrics", 1997, Proceedings, Second Annual IEEE International Conference on Innovative Systems in Silicon 1997) and Landman (Landman, Paul; High-Level Power Estimation", 1996, International Symposium on Low Power Electronics and Design, Proceedings of the 1996 International Symposium on Low Power Electronics and Design) in view of Peschko (Peschko, Ed; DeWolfe, Michele; "Perl 5 Complete", 1998, McGraw-Hill Professional).

21.1. Claim 15 is a dependent claim of claim 14, and thereby inherits all of the rejected limitations of claim 14.

21.2. The art of Peschko is directed to using Perl ***(Title)***.

21.3. Peschko appears to teach that Perl scripts are used for building tools ***(page 44, section: Introduction)***.

21.4. The motivation to combine the art of Peschko with the art of Chen would have been the need in Chen for a programming tool to use to build translate a benchmark program into instructions ***(Chen, page 2, figure 1, Assembler)***, and the solution provided by Perl as a tool builder described in Peschko ***(page 44, section: Introduction)***.

21.5. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Chen and Landman with the art of Peschko to produce the invention of claim 15.

22. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (Chen, Rita Yu; Irwin, Mary Jane; Raminder, S. Bajwa; "An Architectural Level Power Estimator", 1998, ISCA 1998) and Fornaciari (Fornaciari, W.; Gubian, P.; Sciuto, D.; Silvano, C.; "System-Level Power Evaluation Metrics", 1997, Proceedings, Second Annual IEEE International Conference on Innovative Systems in Silicon 1997) and Landman (Landman, Paul; High-Level Power Estimation", 1996, International Symposium on Low Power Electronics and Design, Proceedings of the 1996 International Symposium on Low Power Electronics and Design).

22.1. Claim 16 is a dependent claim of claim 12, and thereby inherits all of the rejected limitations of claim 12.

22.2. Landman appears to teach selecting each of the architectural functions individually ***(section 3 Architecture-level power estimation, and section 3.1.1 Complexity-based models)***, counting a number of technology gates constituting each of the architectural functions ***(section 3.1.1 Complexity-based models, paragraph 1)***, determining a power weight for each gate ***(section 3.1.1 Complexity-based models, paragraph 1, and equation 1)***, and deriving a power weight for each

architectural function ***(section 3.1.1 Complexity-based models, paragraph 1)***.

22.2.1. It is obvious that the characteristic technology is used to determine the power weight for each gate.

22.3. Therefore, as discussed above, it would have been obvious to the ordinary artisan at the time of invention to use the art of Landman and Chen to produce the invention of claim 16.

23. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (Chen, Rita Yu; Irwin, Mary Jane; Raminder, S. Bajwa; "An Architectural Level Power Estimator", 1998, ISCA 1998) and Fornaciari (Fornaciari, W.; Gubian, P.; Sciuto, D.; Silvano, C.; "System-Level Power Evaluation Metrics", 1997, Proceedings, Second Annual IEEE International Conference on Innovative Systems in Silicon 1997) and Landman (Landman, Paul; High-Level Power Estimation", 1996, International Symposium on Low Power Electronics and Design, Proceedings of the 1996 International Symposium on Low Power Electronics and Design).

23.1. Claim 17 is a dependent claim of claim 12, and thereby inherits all of the rejected limitations of claim 12.

23.2. Chen appears to teach running benchmark programs to evaluate power consumption ***(section 3.0 Validation, paragraph 2)***.

23.2.1. Regarding ***(section 3.0 Validation, paragraph 2)***; it would have been obvious to one of ordinary skill in the art at the time of invention to use a power virus as a benchmark program.

24. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (Chen, Rita Yu; Irwin, Mary Jane; Raminder, S. Bajwa; "An Architectural Level Power Estimator", 1998, ISCA 1998) and Fornaciari (Fornaciari, W.; Gubian, P.; Sciuto, D.; Silvano, C.; "System-Level Power Evaluation Metrics", 1997, Proceedings, Second Annual IEEE International Conference on Innovative Systems in Silicon 1997).

24.1. Claim 18 is a dependent claim of claim 11, and thereby inherits all of the rejected limitations of claim 11.

24.2. Chen appears to teach generating a summary of power consumption results for an architecture and its constituent functions ***(figure 5. Power comparison for MAC unit, and section 2.0 Validation, paragraph 2)***.

24.3. Chen appears to teach generating a summary of performance for an architecture ***(figure 4)***.

25. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (Chen, Rita Yu; Irwin, Mary Jane; Raminder, S. Bajwa; "An Architectural Level Power Estimator", 1998, ISCA 1998) and Fornaciari

(Fornaciari, W.; Gubian, P.; Sciuto, D.; Silvano, C.; "System-Level Power Evaluation Metrics", 1997, Proceedings, Second Annual IEEE International Conference on Innovative Systems in Silicon 1997).

25.1. Claim 19 is a dependent claim of claim 11, and thereby inherits all of the rejected limitations of claim 11.

25.2. Chen appears to teach analyzing a summary ***(section 4.0 Architectural Level Trade-offs, first paragraph. In the first paragraph, an analysis of a summary appears to be performed)***.

26. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (Chen, Rita Yu; Irwin, Mary Jane; Raminder, S. Bajwa; "An Architectural Level Power Estimator", 1998, ISCA 1998) and Fornaciari (Fornaciari, W.; Gubian, P.; Sciuto, D.; Silvano, C.; "System-Level Power Evaluation Metrics", 1997, Proceedings, Second Annual IEEE International Conference on Innovative Systems in Silicon 1997).

26.1. Claim 20 is a dependent claim of claim 19, and thereby inherits all of the rejected limitations of claim 19.

26.2. Fornaciari appears to teach analyzing a summary ***(section 2.0 Metric Driven System-Level Partitioning, paragraph 1 and paragraph 2)***.

26.2.1. Regarding ***(section 2.0 Metric Driven System-Level Partitioning, paragraph 1 and paragraph 2);*** the cost function in paragraph 2 balances power and performance (speed).

27. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (Chen, Rita Yu; Irwin, Mary Jane; Raminder, S. Bajwa; "An Architectural Level Power Estimator", 1998, ISCA 1998) and Fornaciari (Fornaciari, W.; Gubian, P.; Sciuto, D.; Silvano, C.; "System-Level Power Evaluation Metrics", 1997, Proceedings, Second Annual IEEE International Conference on Innovative Systems in Silicon 1997).

27.1. Claim 21 is a dependent claim of claim 11, and thereby inherits all of the rejected limitations of claim 11.

27.2. Chen appears to teach the method of claim 11 wherein the architecture is a microprocessor ***(section 3.0 Validation, first paragraph. The 32-bit RISC processor is a microprocessor)***.

28. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (Chen, Rita Yu; Irwin, Mary Jane; Raminder, S. Bajwa; "An Architectural Level Power Estimator", 1998, ISCA 1998) and Fornaciari (Fornaciari, W.; Gubian, P.; Sciuto, D.; Silvano, C.; "System-Level Power Evaluation Metrics", 1997, Proceedings, Second Annual IEEE International Conference on Innovative Systems in Silicon 1997).

28.1. Claim 22 is a dependent claim of claim 11, and thereby inherits all of the rejected limitations of claim 11.

28.2. Chen appears to teach architecture level power evaluation wherein the architecture is an integrated circuit ***(section 3.0 Validation, first paragraph. It is obvious that the 32-bit RISC processor is an integrated circuit because it is on a single chip)***.

29. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (Chen, Rita Yu; Irwin, Mary Jane; Raminder, S. Bajwa; "An Architectural Level Power Estimator", 1998, ISCA 1998) and Fornaciari (Fornaciari, W.; Gubian, P.; Sciuto, D.; Silvano, C.; "System-Level Power Evaluation Metrics", 1997, Proceedings, Second Annual IEEE International Conference on Innovative Systems in Silicon 1997).

29.1. Claim 23 is a dependent claim of claim 22, and thereby inherits all of the rejected limitations of claim 22.

29.2. Fornaciari appears to teach system-level power evaluation using the architecture of an application specific integrated circuit (ASIC) ***(section 1. Introduction, first paragraph, and Abstract. It is obvious that the ASIC is intended to have a power level evaluation)***.

Conclusion

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell L. Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday – Friday 9:00 AM - 5:30 PM Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Any inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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